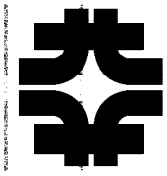

Fermi National Accelerator Laboratory

SVX II Silicon Upgrade

Silicon **R**eadout **C**ontroller

-SRC Transition Module Board Design-
Preliminary Document

5 March, 1998

Harvard University

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1. Introduction

This is a preliminary document. As the design progresses a more complete version will become available.

This document specifies the design of the Silicon Readout Controller Transition Module or SRCTM. The SRCTM is a 9U transition board whose purpose is to transmit commands and data from the SRC to the FIBs at a high rate and to receive FIB errors via a status return cable. To accomplish this the SRCTM uses the HP G-link chip and the Finisar fiber optic Transmitter. The Gigabit rate G-link chip acts as virtual ribbon cable interface. 20 bits of parallel data and commands from the SRC are serialized by the G-link then transmitted to the FIB Fanout through an optical fiber. Each FIB Fanout converts the serial data into parallel using the receiving versions of the same components.

2. Board design

The SRCTM contains Four G-link Optical Transmitters and four FIB Fanout status return cable connections as can be seen in Figure 2-1. SVX requires 4 FIB status return cables. ISL also requires 4 FIB status return. If the same SRC is to control the SVX and ISL the SRCTM would need to provide for 8 FIB Fanouts. This can be accomplished by optically splitting the four G-link fibers into eight. Also, the SRCTM will have connectors for an optional mezzanine card containing an additional four status return connectors. Each of the FIB status lines returned from different fibs will be ORed providing one set of status to the SRC. A block diagram of the SRCTM is given in Figure 2-1.

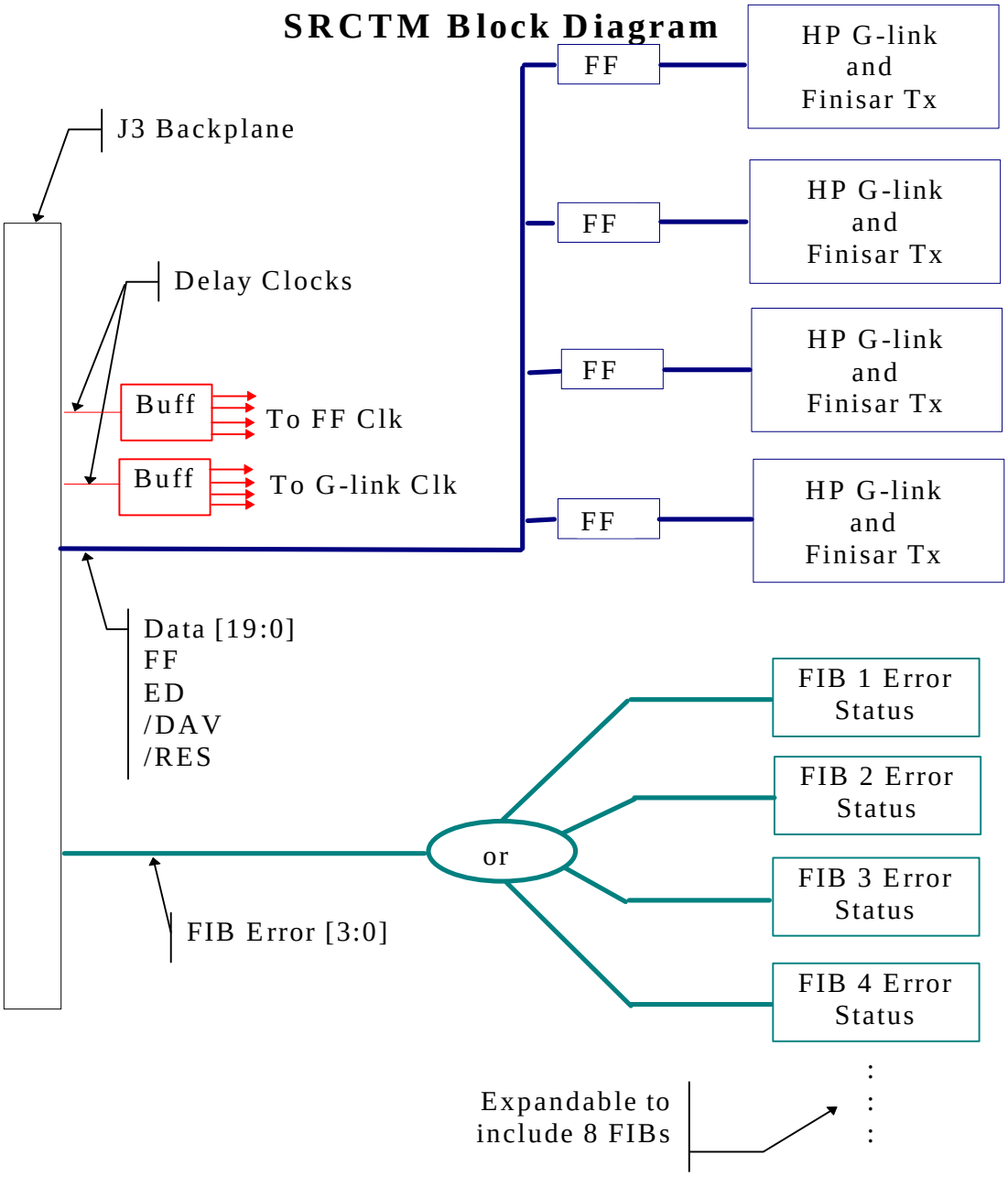


Figure 2-1 - Block Diagram

Figure 2-2 shows how G-link data enters the Board through the backplane from the SRC. Since all of the FIBs will get the same data, one set of data will travel along the board as a bus. The data is registered before going to the G-link circuits. The part chosen for the registers (CY74FCT2374) incorporates a series resistor to reduce reflection noise.

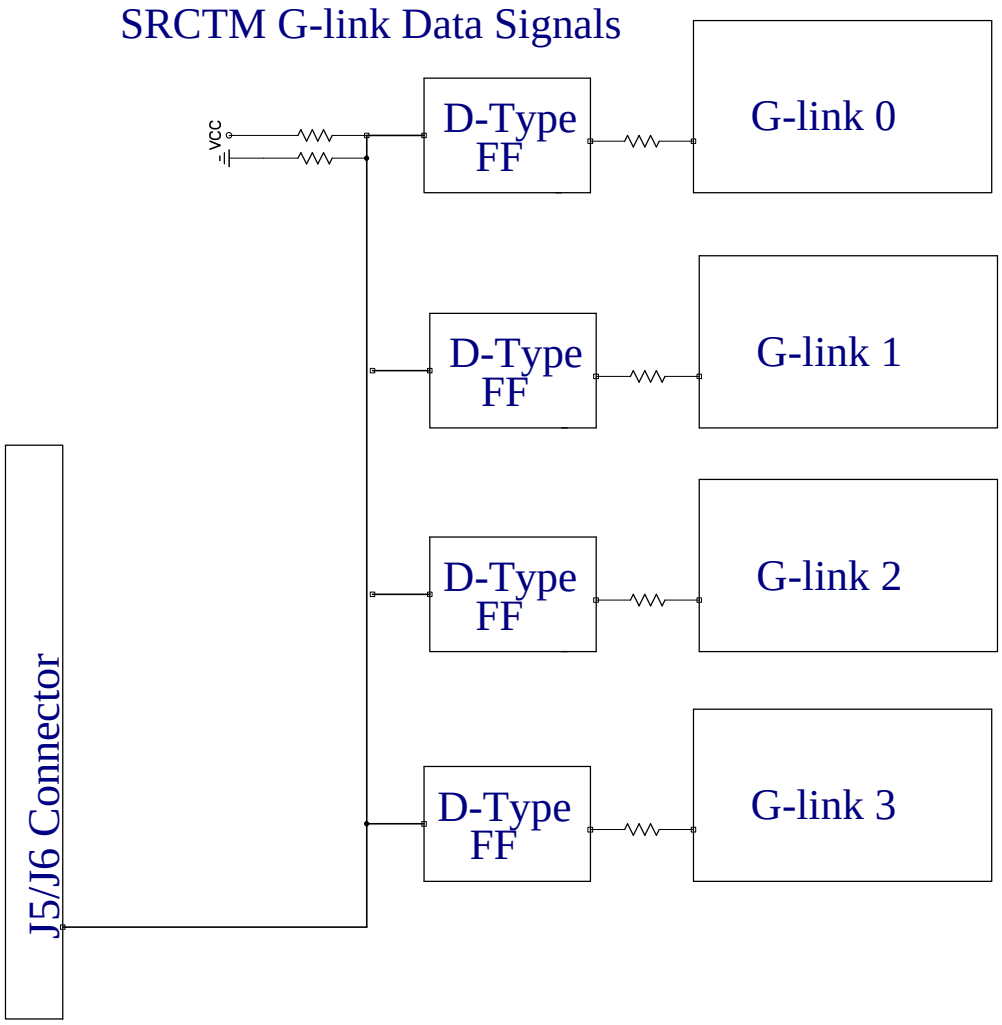


Figure 2-2 - Board Data Bus

The board requires two clocks, one for the G-links and one for the registers. These clocks are adjustable on the SRC. The clocks are split and buffered close to the connector as seen in Figure 2-3. The signals are terminated and buffered once more before the G-link and register clock input. The part chosen for the buffers (CY74FCT2244) incarcerate a series resistor to reduce reflection noise.

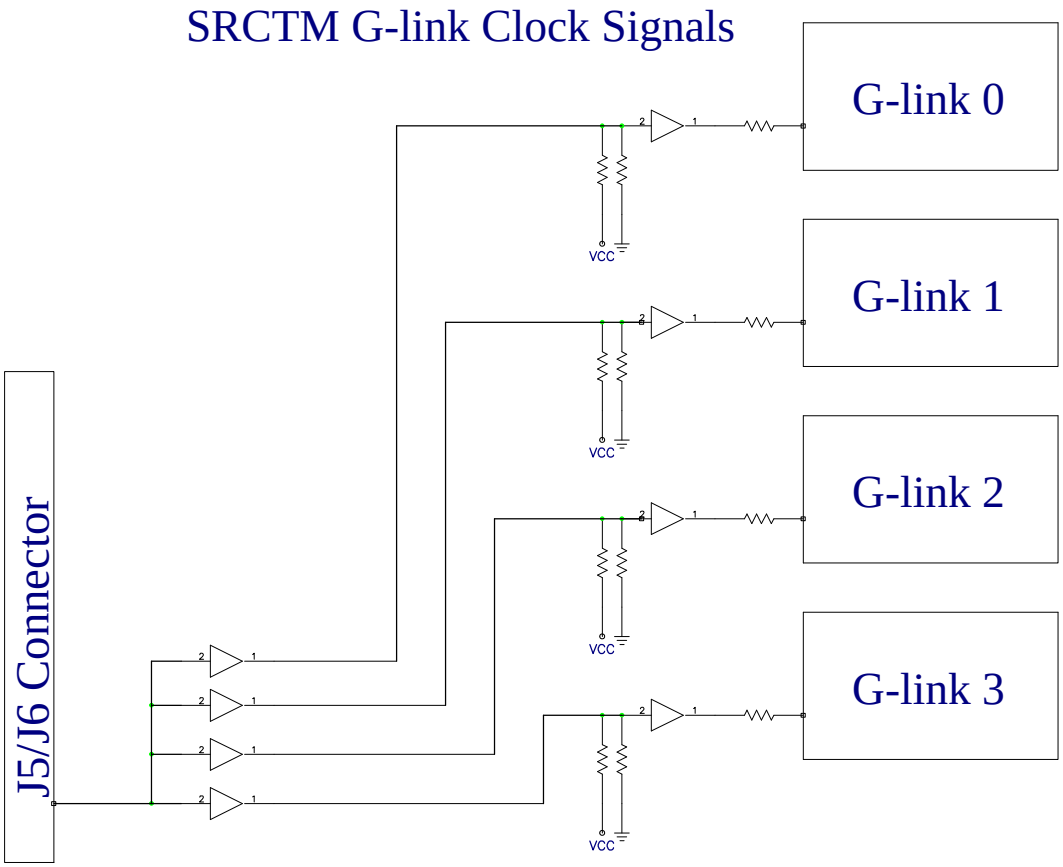
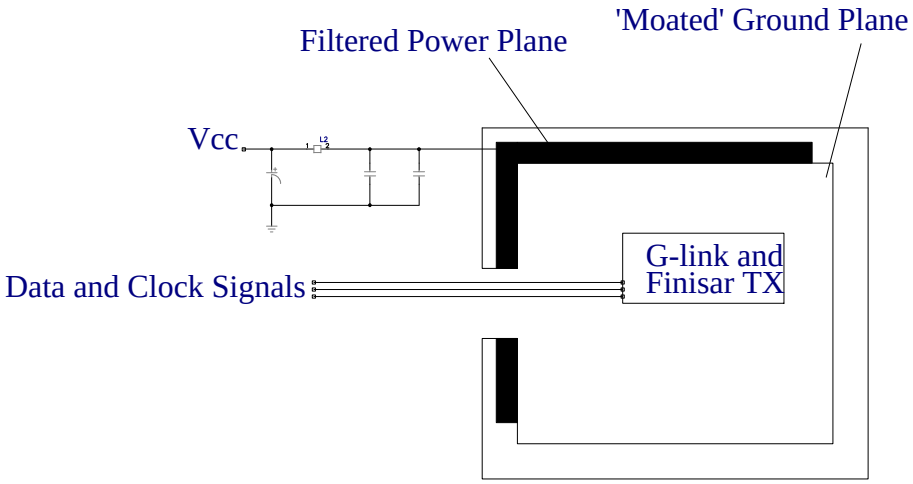


Figure 2-3 - Board Clocks

Each G-link and Finisar transmitter pair will have their own filtered power plane and moated ground plane shown in Figure 2-4. The data signals and clock will cross the Moat over the portion of the ground plane which is connected to the board plane.

SRCTM Power and Ground Planes



Every G-link and Finisar Optical Part will have a Filtered Power

Figure 2-4 - G-link Power and Ground

3. Physical Description

The SRCTM is 366.7 mm tall, 120mm wide and .093 inch thick. the board will is milled to 0.063" along the top and bottom solder side. as seen in Figure 3-1 the board has 6 layers, four layers are signal layers and two are power layers. The top and bottom signal micro strip layers are 13.5 mills wide and have an impedance of 77 ohms. All of the high speed signals like the data bus and the clock lines are routed on the top and bottom layers

Top Signal Layer ____
Power Layer _____
Signal Layer _ _ _
Signal Layer ____
Ground Layer _____
Bottom Signal Layer _ _ _

Figure 3-1 Board layers

4. Appendix

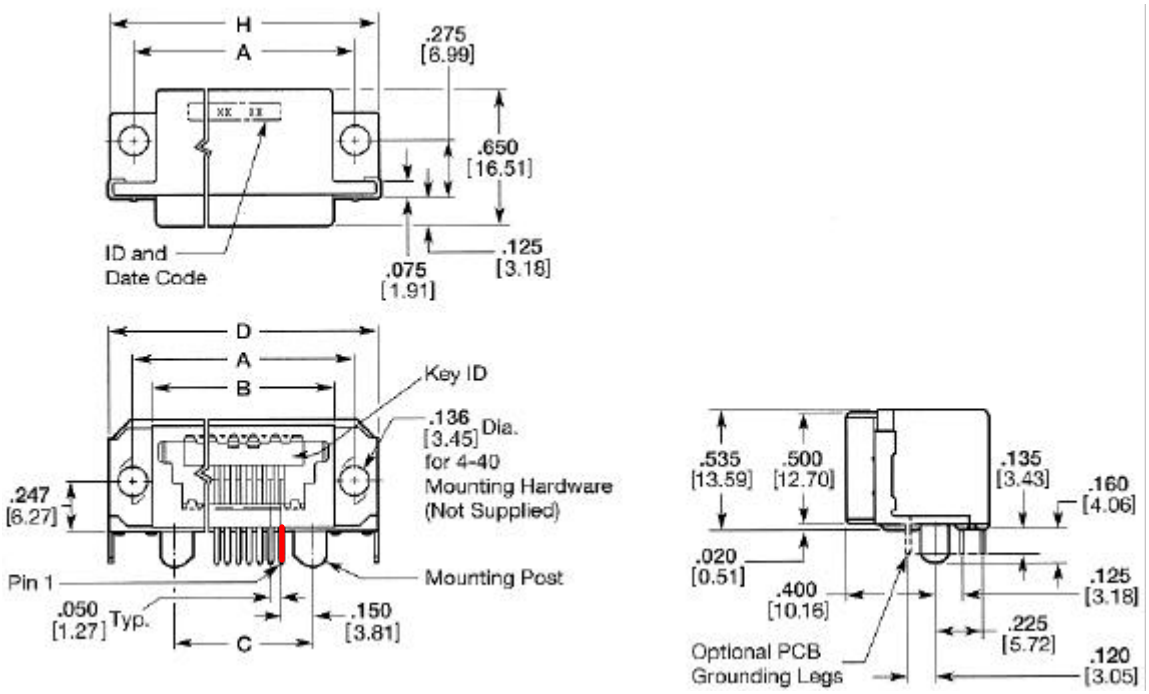


Figure 4-1 - FIB Status Return Cable Connector

Pin	Signal
1	FIB_ER0+
2	FIB_ER0-
3	FIB_ER1+
4	FIB_ER1-
5	FIB_ER2+
6	FIB_ER2-
7	FIB_ER3+
8	FIB_ER3-

Figure 4-2 - FIB Status Cable Pinouts

Mezzanine Connector A

Pin	Signal
1	FIB4_ER0+
2	FIB4_ER0-
3	FIB4_ER1+
4	FIB4_ER1-
5	FIB4_ER2+
6	FIB4_ER2-
7	FIB4_ER3+
8	FIB4_ER3-
9	FIB5_ER3-
10	FIB5_ER3+
11	FIB5_ER2-
12	FIB5_ER2+
13	FIB5_ER1-
14	FIB5_ER1+
15	FIB5_ER0-
16	FIB5_ER0+

Mezzanine Connector B

Pin	Signal
1	FIB6_ER0+
2	FIB6_ER0-
3	FIB6_ER1+
4	FIB6_ER1-
5	FIB6_ER2+
6	FIB6_ER2-
7	FIB6_ER3+
8	FIB6_ER3-
9	FIB7_ER3-
10	FIB7_ER3+
11	FIB7_ER2-
12	FIB7_ER2+
13	FIB7_ER1-
14	FIB7_ER1+
15	FIB7_ER0-
16	FIB7_ER0+

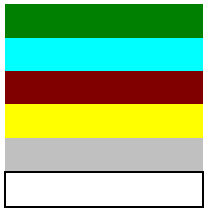
Figure 4-3 - Optional Mezzanine Connector for FIB 3-7

Design					SRCTM J3 Connector Connections
Date					2/2/98 14:18
Signal	**I**	**O**	**OT**	**I/O**	**Function**
GLD[19:0]	20				G-link Data (20 Bits)
FF	1				Fill Frame
/RES	1				Reset
/DAV	1				Data Valid
ED	1				Enable Data
/CAV	1				Command Valid (used to signal FFO RUN)
LOCK		1			G-link Transmitter Lock With RF_CLK
FIB_ERR[3:0]		4			FIB Fanout Error Return Line
/CS[3:0]	4				G-link Status chip select
SI	1				G-link Status Serial Command Input
SO		1			G-link Status Serial Data Output
READY		1			G-link Status Ready
SCLK	1				G-link Status Clock
GL_CLOCK	1				Phase Adjustable CDF 53MHz Clock
RF_DEL_CLK	1				Phase Adjustable CDF 53MHz Clock
Pin Count	**33**	**7**	**0**	**0**	**40**

Figure 4-4 - J5/J6 Signals

PIN	ROW A	ROW B	ROW C	ROW D	ROW E	ROW F
1	GND	FIB CLK	TTL0	FIB CLK	GND	GND
2	B_MCLK	FIB CLK	TTL1	FIB CLK	GND	GND
3	GND	FIB CLK	TTL2	FIB CLK	GND	GND
4	B_AD_PIPE	FIB CLK	TTL3	FIB CLK	GND	GND
5	GND	FIB CLK	TTL4	FIB CLK	GND	GND
6	B_SYNC	FIB CLK	TTL5	FIB CLK	GND	GND
7	GND	FIB CLK	TTL6	FIB CLK	GND	GND
8	GND	FIB CLK	TTL7	FIB CLK	GND	GND
9	GND	FIB CLK	TTL8	FIB CLK	GND	GND
10	GND	FIB CLK	TTL9	FIB CLK	GND	GND
11	GND	FIB CLK	TTL10	FIB CLK	GND	GND
12	GND	FIB CLK	TTL11	FIB CLK	GND	GND
13	GND	FIB CLK	TTL12	FIB CLK	GND	GND
14	***RF_DEL_CLK***	FIB CLK	TTL13	FIB CLK	GND	GND
15	GND	FIB CLK	TTL14	FIB CLK	GND	GND
16	**GL_CLK**	FIB CLK	TTL15	FIB CLK	GND	GND
17	GND	FIB CLK	TTL16	FIB CLK	GND	GND
18	C0	FIB CLK	TTL17	FIB CLK	GND	GND
19	**/RESET**	FIB CLK	TTL18	FIB CLK	GND	GND
20	C1	FIB CLK	TTL19	FIB CLK	GND	GND
21	**FF**	FIB CLK	TTL20	FIB CLK	GND	GND
22	C2	FIB CLK	TTL21	FIB CLK	GND	GND
23	GND	FIB CLK	TTL22	FIB CLK	GND	GND
24	C3	FIB CLK	TTL23	FIB CLK	GND	GND
25	GND	GND	TTL24	GND	GND	GND
26	C4	**READY**	GND	GND	**/CS0**	GND
27	**S1**	**SCLK**	GND	**/CS2**	**/CS1**	GND
28	C5	**S0**	GND	**/CS3**	GND	GND
29	GND	GND	GND	GND	**/CAV**	GND
30	L_1/0	GND	GND	GND	GND	GND
31	GND	**FIB_ERR0**	GND	**ED**	GND	GND
32	C_CLK1	**FIB_ERR1**	N/C	**/DAV**	**LOCK**	GND
33	GND	**FIB_ERR2**	GND	GND	GND	GND
34	C_CLK2	**FIB_ERR3**	GND	GND	GND	GND
35	**GLD18**	GND	GND	GND	**GLD19**	GND
36	PIPE_RD2	**GLD16**	GND	**GLD17**	GND	GND
37	GND	GND	GND	GND	GND	GND
38	L1A	**GLD14**	GND	**GLD15**	GND	GND
39	**GLD12**	GND	GND	GND	**GLD13**	GND
40	FE_CLK1	**GLD10**	GND	**GLD11**	GND	GND
41	GND	GND	GND	GND	GND	GND
42	FE_CLK2	**GLD8**	GND	**GLD9**	GND	GND
43	**GLD6**	GND	GND	GND	**GLD7**	GND
44	BE_CLK1	**GLD4**	GND	**GLD5**	GND	GND
45	GND	GND	GND	GND	GND	GND
46	BE_CLK2	**GLD2**	GND	**GLD3**	GND	GND
47	**GLD0**	GND	GND	GND	**GLD1**	GND

REVISED LAYOUT for use with FFO and SRC and DEM



Pins for FFO to DEM interface; N/C on SRC & SRCTM
Pins for FFO to FIB or VFO to VRB or SRC to VRB interface
Pins for FFO/SRC to SRCTM interface
Pins for FFO to FIB clock distribution
Pins for FFO/VFO to termination power distribution
Free pins

Figure 4-5 - J5/J6 Connector Pinouts

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